Listing of Claims

The below listing of claims replaces all other prior versions of claims.

1. (cancelled)

2. (cancelled)

3. (currently amended) A monolithic integrated circuit comprising a plurality of logic gates, a single logic gate comprising:

a P-type well formed in an N-type region, the P-type well forming a base of an NPN bipolar transistor;

an N+ region formed in the P-type well forming an emitter of the bipolar transistor;

the N-type region forming a collector of the transistor in common with the cathodes of two or more Schottky diodes;

nodes of the logic gate being adapted for coupling to nodes of other similar logic gates, the nodes of the logic gate comprising an input node coupled to the base and comprising output nodes coupled to respective anodes of the two or more Schottky diodes,

wherein the two or more Schottky diodes comprise one or more output Schottky diodes and at least one clamping Schottky diode, the at least one clamping Schottky diode being coupled between the collector and base of the transistor; and

~~The circuit of Claim 2 further comprising~~ a resistor in series with the at least one clamping Schottky diode,

wherein an anode metal of all the Schottky diodes comprises titanium or titanium silicide.

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4. (currently amended) The circuit of Claim ~~2~~ 5 wherein an anode metal of the at least one clamping Schottky diode comprises titanium or titanium silicide.

5. (currently amended) A monolithic integrated circuit comprising a plurality of logic gates, a single logic gate comprising:

a P-type well formed in an N-type region, the P-type well forming a base of an NPN bipolar transistor;

an N+ region formed in the P-type well forming an emitter of the bipolar transistor;

the N-type region forming a collector of the transistor in common with the cathodes of two or more Schottky diodes; and

nodes of the logic gate being adapted for coupling to nodes of other similar logic gates, the nodes of the logic gate comprising an input node coupled to the base and comprising output nodes coupled to respective anodes of the two or more Schottky diodes,

wherein the two or more Schottky diodes comprise one or more output Schottky diodes and at least one clamping Schottky diode, the at least one clamping Schottky diode being coupled between the collector and base of the transistor,

~~The circuit of Claim 2~~ wherein there are two or more Schottky diodes connected in series between the collector and base of the transistor.

6. (currently amended) The circuit of Claim 5 wherein an anode metal of at least one of the two or more Schottky diodes connected in series comprises aluminum, titanium, platinum, or silicides of those metals.

7. (currently amended) The circuit of Claim ~~1~~ 5 wherein the N-type region is a portion of an N-type epitaxial layer, the portion being electrically isolated from other portions of the epitaxial layer.

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8. (currently amended) The circuit of Claim ~~1~~ 5 wherein the N-type region is an N-type well formed within a P-type material.

9. (currently amended) The circuit of Claim ~~1~~ 5 further comprising an anode metal of each of the two or more Schottky diodes in contact with the N-type region.

10. (original) The circuit of Claim 9 wherein the anode metal of at least one Schottky diode comprises aluminum or aluminum silicide.

11. (original) The circuit of Claim 9 wherein the anode metal of at least one Schottky diode comprises platinum or platinum silicide.

12. (original) The circuit of Claim 9 wherein the anode metal of at least one Schottky diode comprises titanium or titanium silicide.

13. (currently amended) The circuit of Claim ~~1~~ 5 wherein the logic gate forms a portion of a NAND function.

14. (currently amended) The circuit of Claim ~~1~~ 5 wherein anodes of the two or more Schottky diodes are coupled to respective bases of additional NPN bipolar transistors.

15 (currently amended) The circuit of Claim ~~1~~ 5 further comprising multiple logic gates being interconnected such that anodes of the two or more Schottky diodes are coupled to respective bases of bipolar transistors via one or more metal layers.

16. (new) The circuit of Claim 5 wherein an anode metal of all the Schottky diodes comprises titanium or titanium silicide.

17. (new) The circuit of Claim 3 wherein the N-type region is a portion of an N-type epitaxial layer, the portion being electrically isolated from other portions of the epitaxial layer.

18. (new) The circuit of Claim 3 further comprising an anode metal of each of the two or more Schottky diodes in contact with the N-type region.

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19. (new) The circuit of Claim 3 wherein an anode metal of all the Schottky diodes consists solely of titanium or titanium silicide.

20. (new) The circuit of Claim 3 further comprising multiple logic gates being interconnected such that anodes of the two or more Schottky diodes are coupled to respective bases of bipolar transistors via one or more metal layers.

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